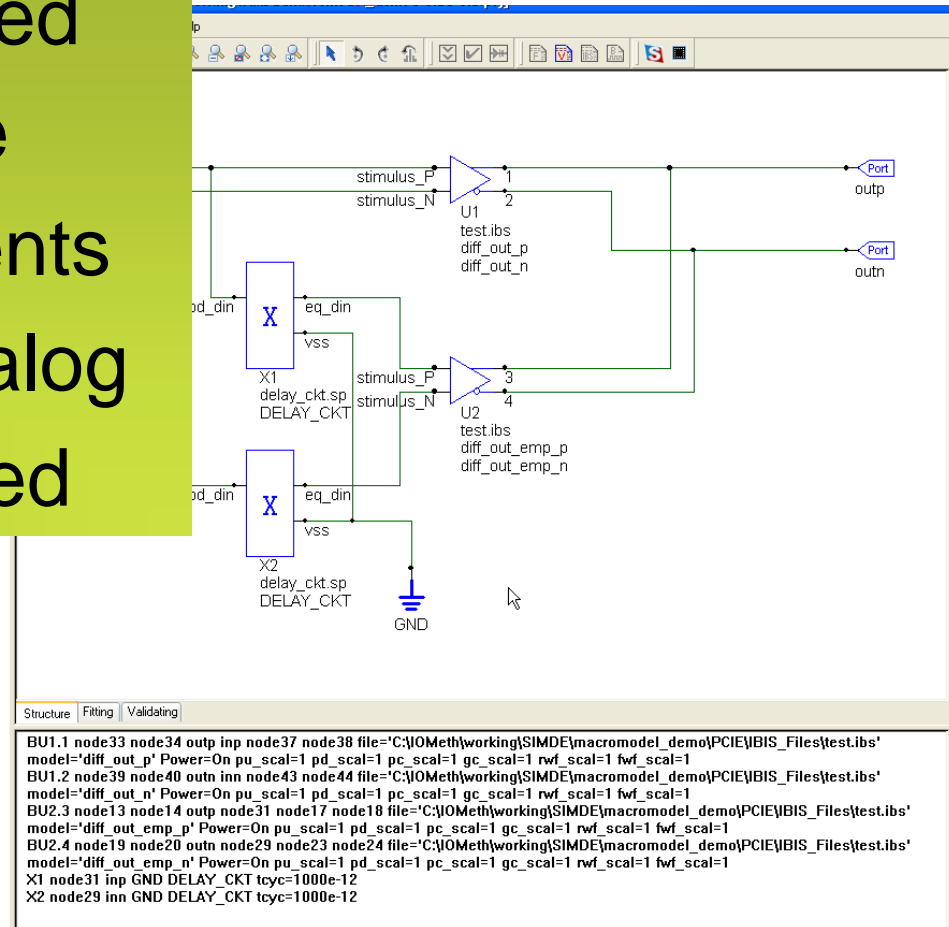

Spice Macromodeling Advantages for Advanced I/O Buffers

With a Giga-Hertz pre-
emphasis driver example



What is the Spice Macromodel?

- Spice syntax based
- Modular structure
- Behavioral elements
- Digital or/and Analog
- Schematic oriented



Advantages of Spice Macromodel

- **Advanced modeling for new technologies**
 - Pre-emphasis models
 - SSO/SSN models
 - Digital Pattern generator
 - Analog models
- **Digital or Analog or Mixed**
 - Modeling with digital and analog blocks together
- **IP protected**
 - Behavioral schematic only. No physical detail exposed.
- **Performance for what-if analysis**
 - Up to 850+ times faster than transistor-level model simulations
- **No extra cost for users (with existing Spice simulator)**
 - Uses existing Spice syntax

Example

- 2 tap pre-emphasis GHz driver

■ Original

- Model

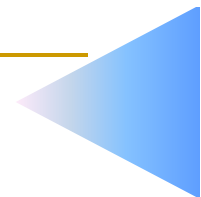
- HSpice transistor-level model
- 12 netlist and library files total 3.56MB file size;

- Computer

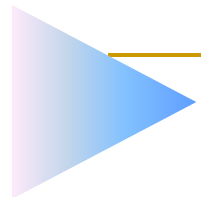
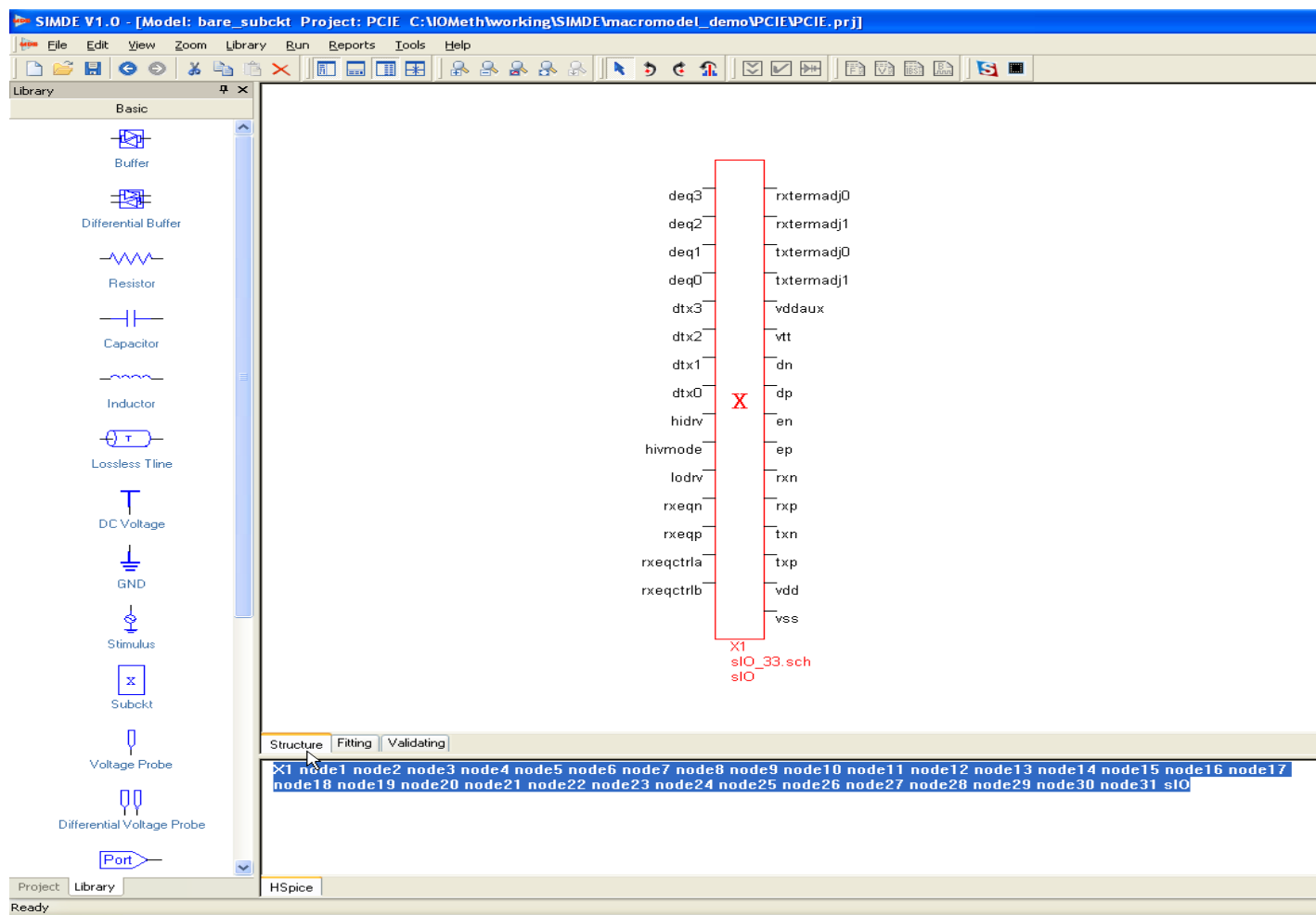
- 2.1GHz Duo-Core, 2GHz RAM, WinXP

- Simulation

- PRBS 640 bits@2.5Gbps
- 16 inch channel (S-parameter)
- 22 hours



Example - Top subckt



Example

- IBIS extraction for MAIN and BOOST drivers

The image shows a circuit schematic on the left and a configuration dialog box on the right. The schematic includes a central component 'X1' with various pins connected to nodes like 'deq3', 'deq2', 'deq1', 'deq0', 'db3', 'db2', 'db1', 'db0', 'hidnv', 'hivmode', 'lodnv', 'nceqn', 'nceqp', 'nceqtrila', 'nceqtrilb', 'vddaux', 'vtt', 'dn', 'dp', 'en', 'ep', 'ncn', 'ncp', 'bn', 'bp', 'vdd', and 'vss'. It also shows voltage sources 'V1 DC = \$vddval' and 'V2 DC = 1V' connected to the circuit.

The 'IBIS Diff Buffer Generation Setting' dialog box is configured as follows:

- Node Mapping:**
 - 1 - Stimulus: dp
 - 2 - Pad: txp
 - 3 - Pullup: vtt
 - 4 - Power Clamp: NA
 - 5 - Pulldown: vss
 - 6 - Ground Clamp: NA
 - 7 - Enable: NA
 - 8 - Stimulus_N: dn
 - 9 - Pad_N: txn
- Reference Voltages (V):**

	Typical	Minimum	Maximum
Pullup	1.5		
Pulldown	0		
Power Clamp	1.5		
Ground Clamp	0		
- Model Header:**
 - Model Type: Output
 - vin(V):
 - vinh(V):
 - vmeas(V): 0.75
 - vref(V): 0.75
 - Cref(pF): 15
 - Rref(ohm): 50

At the bottom of the dialog box, there are 'Cancel' and 'Next >>' buttons.

Example

- Build Schematic with swappable parameters

The image shows a circuit schematic in a simulator window. The schematic includes two delay blocks (X1 and X2), two comparators (U1 and U2), two capacitors (C1 and C2), and two resistors (R1 and R2). The components are interconnected with ports (inp, inn, outp, outn) and a ground connection. The parameter editor dialog is open, showing a table of parameters:

Name	Value	Start	Stop	Step
\$C1		0.1p	2.0p	
\$C2		0.1p	2.0p	
\$pd1		0.5	1.5	
\$pu1		0.4	1.6	0.1
\$R1		25	125	5
\$R2		25	125	5
\$V1		0.2	1.7	0.1

Below the schematic, the following text is displayed:

```
BU1.2 node39 node40 outn inn node43 node44 file='C:\IOMeth\working\SIMDE\macromodel_demo\PCIE\IBIS_Files\test.ibs'  
model='diff_out_n' Power=On pu_scal=pu1 pd_scal=pd1 pc_scal=1 gc_scal=1 rwf_scal=1 fwf_scal=1  
BU2.3 node13 node14 outp node31 node17 node18 file='C:\IOMeth\working\SIMDE\macromodel_demo\PCIE\IBIS_Files\test.  
model='diff_out_emp_p' Power=On pu_scal=1 pd_scal=1 pc_scal=1 gc_scal=1 rwf_scal=1 fwf_scal=1  
BU2.4 node19 node20 outn node29 node23 node24 file='C:\IOMeth\working\SIMDE\macromodel_demo\PCIE\IBIS_Files\test.  
model='diff_out_emp_n' Power=On pu_scal=1 pd_scal=1 pc_scal=1 gc_scal=1 rwf_scal=1 fwf_scal=1  
X1 node31 inp GND DELAY_CKT tcyc=800e-12  
X2 node29 inn GND DELAY_CKT tcyc=800e-12
```

Example - Fitting

The screenshot displays a circuit simulation environment. The main window shows a circuit diagram with a voltage source V1, a model component X1 (Model1.mdl), and a resistor R1 (R = 100ohm). A probe labeled 'probe1' is connected to the output nodes of the circuit. An inset window titled 'Fitting Report - Model: Model1' displays a table of fitting parameters for the model.

ID	Probe	DAI(%)	DPI(%)	DA	DP	\$pd1	\$pu1
0	probe1	9.87	11.60	0.05	0.06	0.4	1.05
1	probe1	6.29	7.22	0.03	0.04	1.5	1.05
2	probe1	1.47	2.02	0.01	0.01	1.06	1.05
3	probe1	3.67	4.23	0.02	0.02	1.24	1.05
4	probe1	2.36	2.91	0.01	0.02	1.13	1.05
5	probe1	1.85	2.41	0.01	0.01	1.09	1.05
6	probe1	1.59	2.15	0.01	0.01	1.07	1.05
7	probe1	5.82	7.83	0.03	0.04	1.06	0.6
8	probe1	6.64	7.49	0.04	0.04	1.06	1.5
9	probe1	0.24	0.45	0.00	0.00	1.06	0.96

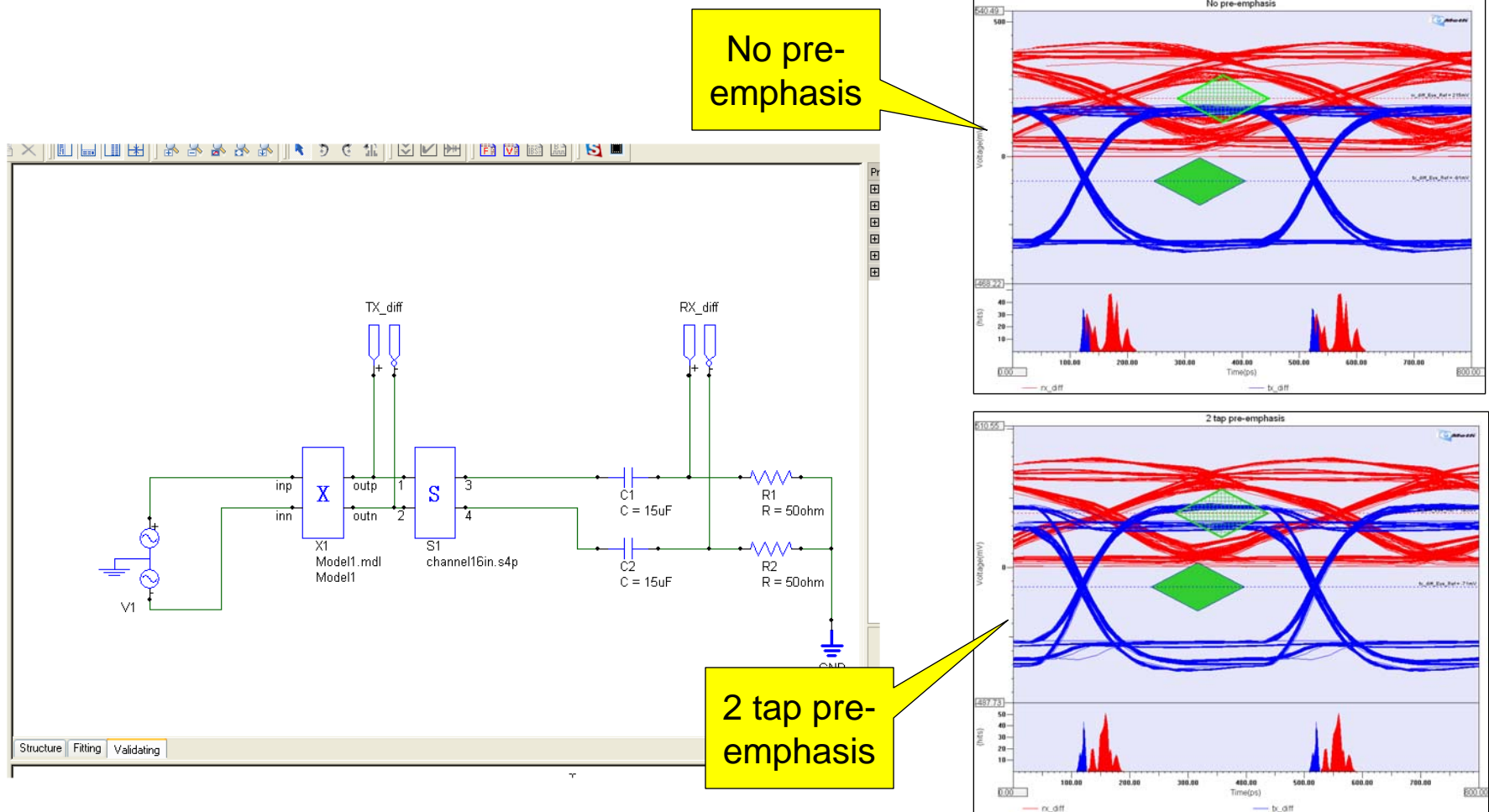
Structure Fitting Validating

```

X1 node1 node2 node7 node8 Model1 pd1=pd1 pu1=pu1
R1 node7 node8 R=100
V1.+ node1 GND CUSTOMISED
V1.- node2 GND CUSTOMISED
  
```


Example

- Validate and do What-if with channel



Example

- Result (DAI: < 5%)

- Spice Macromodel

- Models

- 2 files, 1 HSpice netlist and 1 IBIS file, 200k file size

- Computer

- 2.1GHz Duo-Core, 2G RAM, WinXP

- Simulation

- PRBS 640 bits@2.5Gbps

- 16 inch channel (black box)

- 7 minutes

154 times faster, less than 5% DAI ratio

DAI: Differential Average Index

SIMDE™ V1.0 can help. Set up an evaluation now!

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