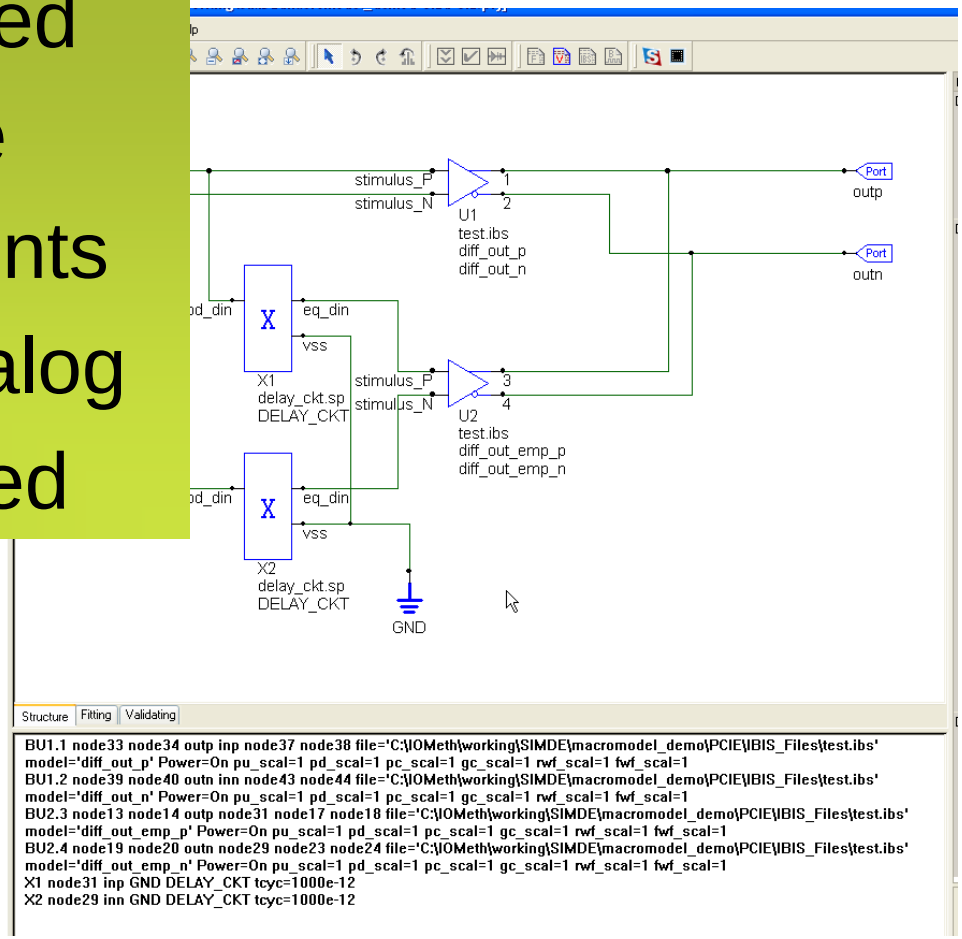
Spice Macromodeling Advantages for Advanced I/O Buffers

With a Giga-Hertz pre-emphasis driver example

What is the Spice Macromodel?

- Spice syntax based
- Modular structure
- Behavioral elements
- Digital or/and Analog
- Schematic oriented



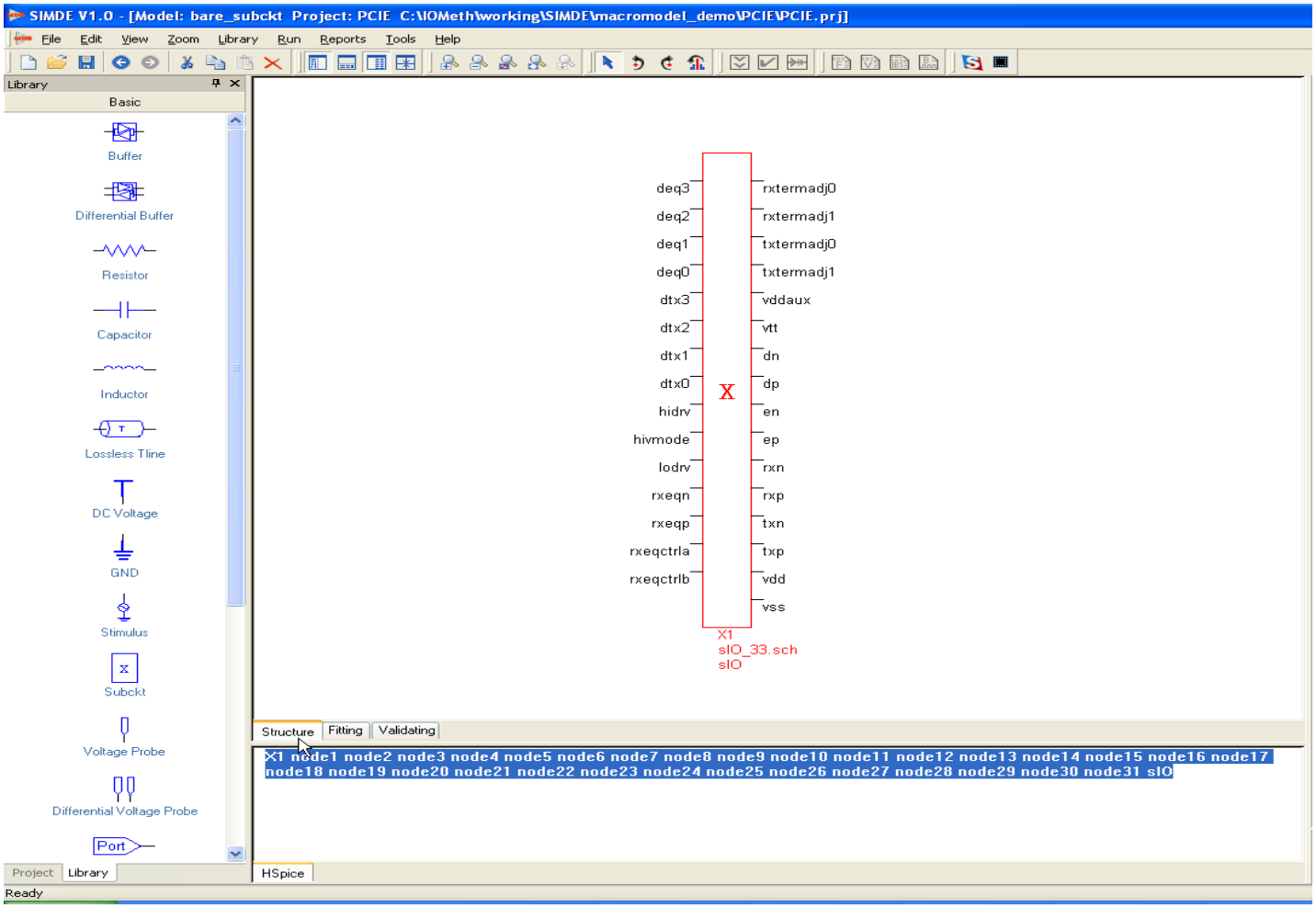
Advantages of Spice Macromodel

- **Advanced modeling for new technologies**
  - Pre-emphasis models
  - SSO/SSN models
  - Digital Pattern generator
  - Analog models
- **Digital or Analog or Mixed**
  - Modeling with digital and analog blocks together
- **IP protected**
  - Behavioral schematic only. No physical detail exposed.
- **Performance for what-if analysis**
  - Up to 850+ times faster than transistor-level model simulations
- **No extra cost for users (with existing Spice simulator)**
  - Uses existing Spice syntax

Example
- 2 tap pre-emphasis GHz driver

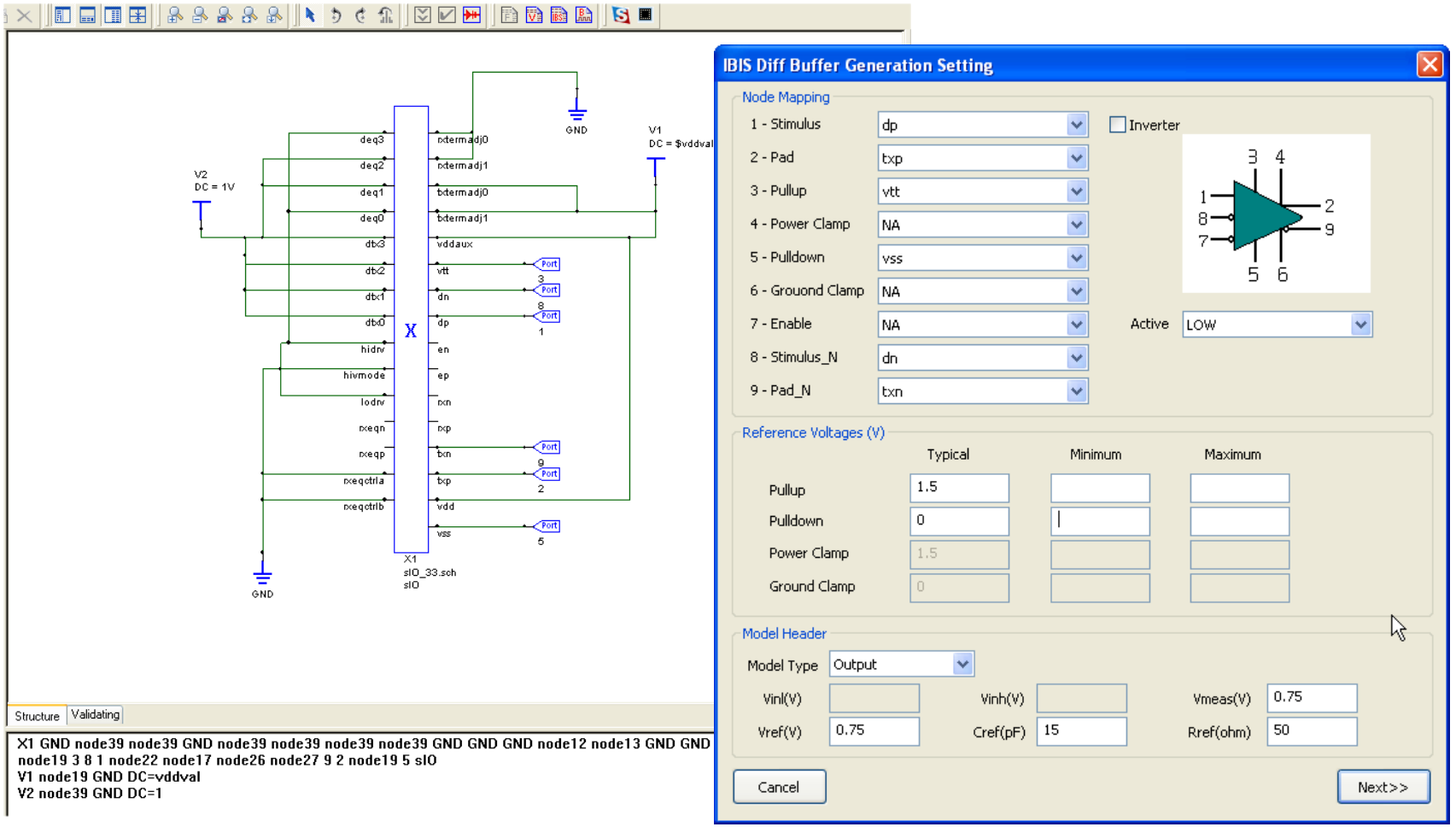
- Original
  - Model
    - HSpice transistor-level model
    - 12 netlist and library files total 3.56MB file size;
  - Computer
    - 2.1GHz Duo-Core, 2GHz RAM, WinXP
  - Simulation
    - PRBS 640 bits@2.5Gbps
    - 16 inch channel (S-parameter)
    - 22 hours

Example
- Top subckt



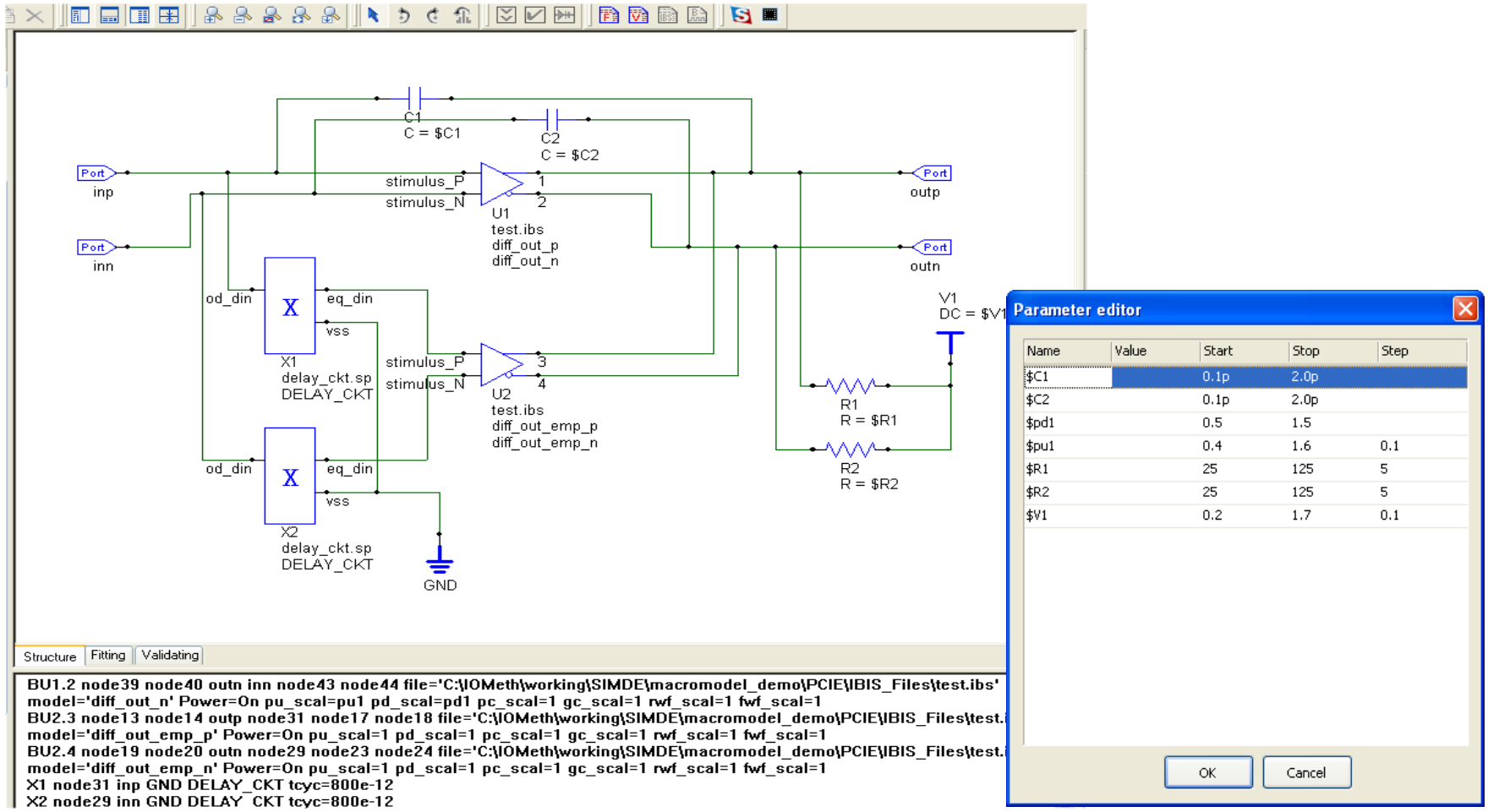
Example

- IBIS extraction for MAIN and BOOST drivers

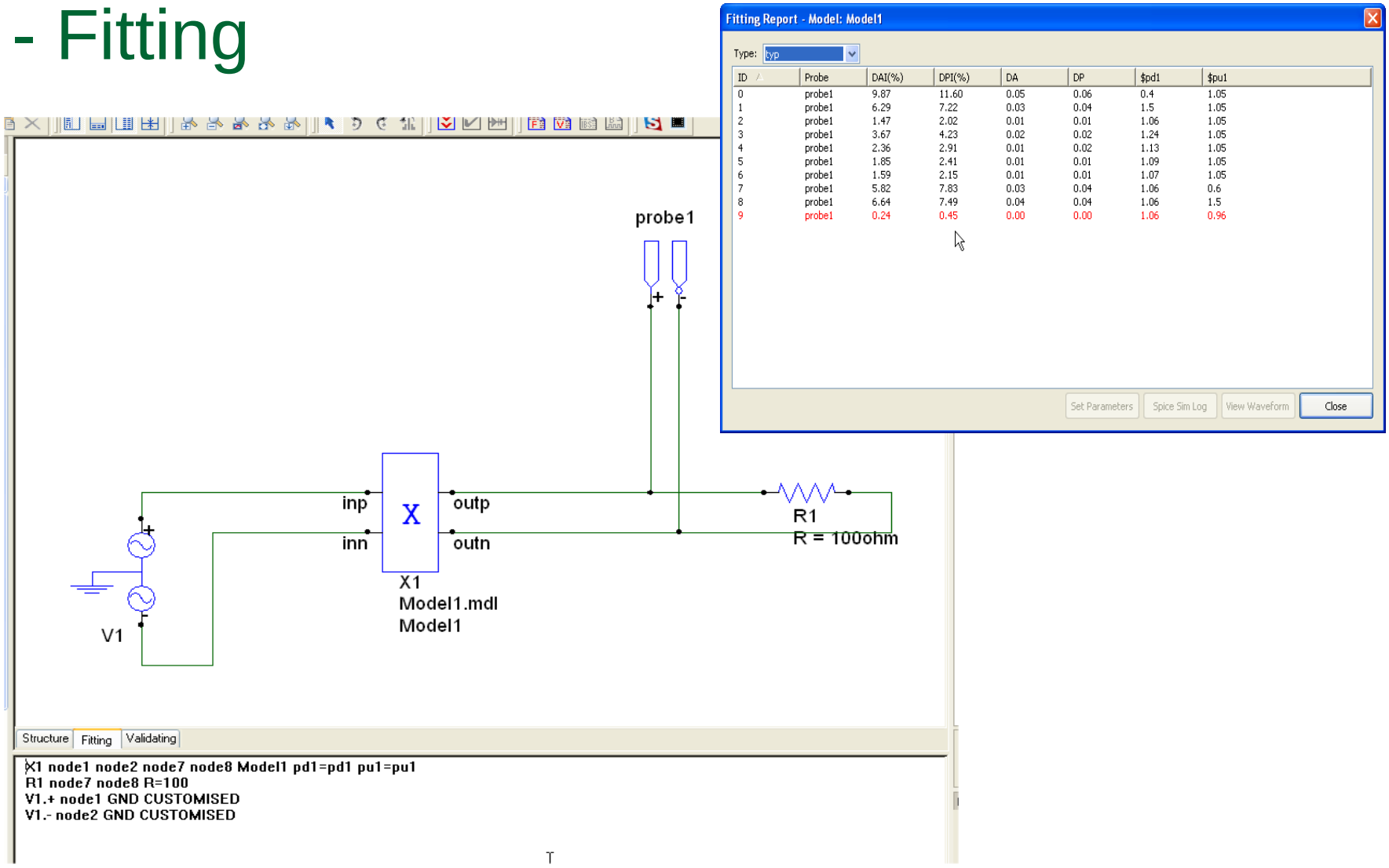


Example

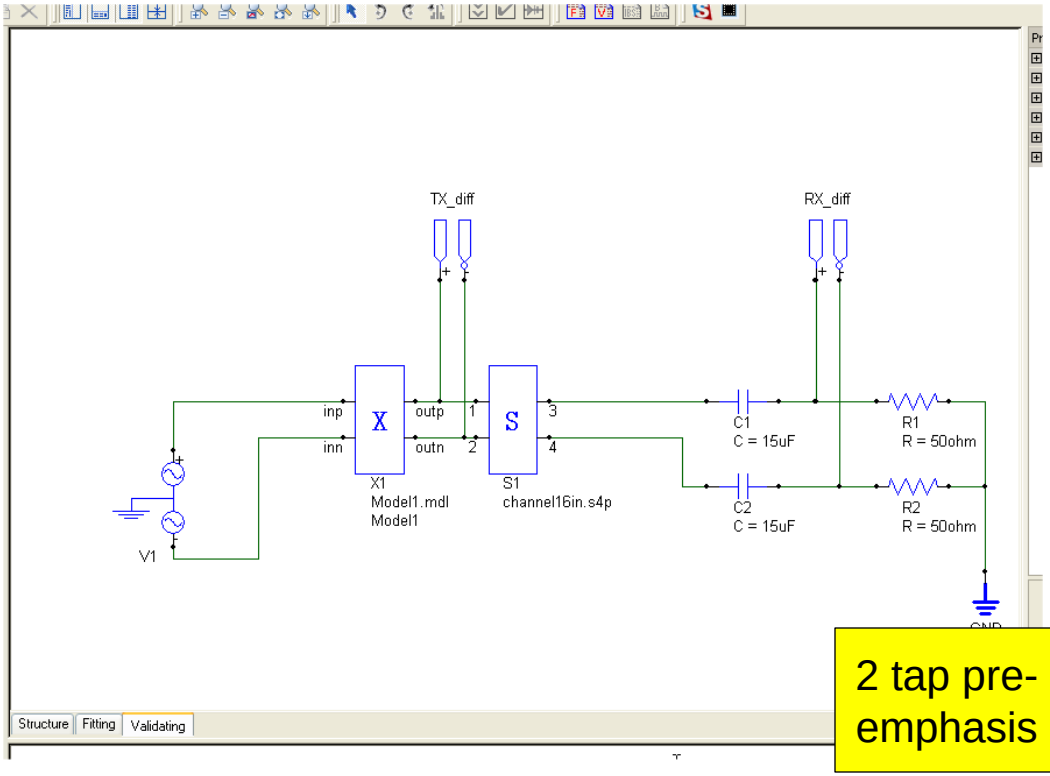
- Build Schematic with swappable parameters



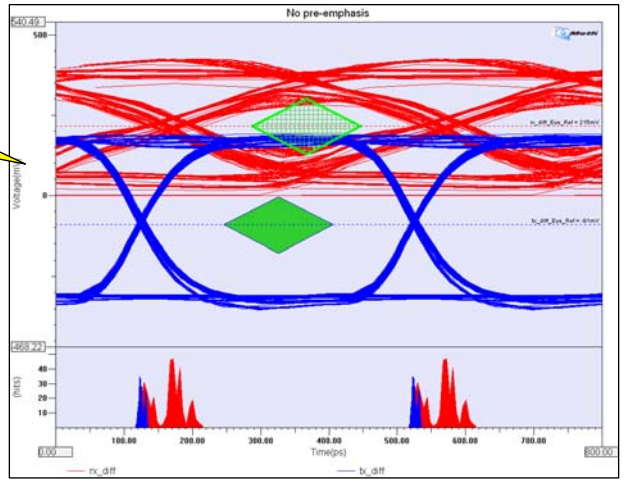
Example
- Fitting



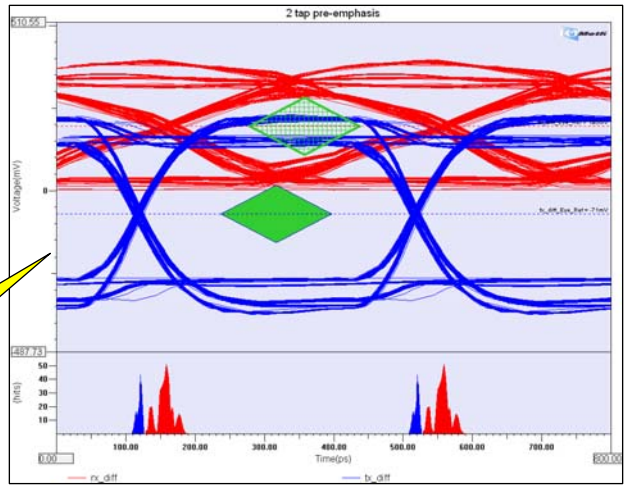
Example
- Validate and do What-if with channel



No pre-emphasis



2 tap pre-emphasis



Example
- Result (DAI: < 5%)

- Spice Macromodel
  - Models
    - 2 files, 1 HSpice netlist and 1 IBIS file, 200k file size
  - Computer
    - 2.1GHz Duo-Core, 2G RAM, WinXP
  - Simulation
    - PRBS 640 bits@2.5Gbps
    - 16 inch channel (black box)
    - 7 minutes

154 times faster, less than 5% DAI ratio

DAI: Differential Average Index

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